



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,993	12/03/2003	Ryosuke Usui	65933-061	5205

20277 7590 02/03/2006

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER

LAM, CATHY FONG FONG

ART UNIT PAPER NUMBER

1775

DATE MAILED: 02/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/725,993	Applicant(s) USUI ET AL.	
	Examiner Cathy Lam	Art Unit 1775	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 7-16 and 22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 17-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11-30-2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

In view of the amendment and remarks filed on November 30, 2005, the objection of the Drawings has been withdrawn. The pending claims however continue to be unpatentable as following:

Election/Restrictions

1. This application contains claims 7-16 and 22 are drawn to an invention nonelected with traverse in Paper No. filed on June 23, 2005. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 102

2. Claims 1, 3-4, 6, 17 and 19-20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Zussman (US 4601944).

Zussman teaches a multilayer printed wiring board comprised of a plurality of prepregs and copper foils (col 6 L 13-21). The examiner takes the position that the prepregs are equivalent to the claimed insulating resin layers and the copper foils would form into wiring patterns.

The prepreg is comprised of a porous substrate and an organic resin (col 2 L 29-30). The organic resin can be epoxy resin or bismaleimide triazine (col 2 L 43-46 & col 1 L 68).

The porous substrate is a polybutadiene material (col 2 L 10-12). The porous material impregnated with epoxy resin would give a dielectric constant of 3.0 or less, if impregnated with bismaleimide triazine would give a dielectric constant of 3.2 or higher

Art Unit: 1775

(col 2 L 8-14 & col 1 L 68-col 2 L 2). Conventional polybutadienes has a dielectric loss tangent of below 10^{-4} (i.e. 0.0010) (col 1 L 35-36).

The polybutadiene is added to the epoxy resin or BT resin to obtain a desirable glass temperature as well as laminate properties. In the table of column 7, laminate A refers to the resin layer that is a 100% polybutadiene which has a dielectric constant of 3.1-3.9 and a tan loss of 0.1-0.5% (i.e. 0.001-0.005). Laminates D, E & H, refer to a resinous composition for an insulating layer that *includes* polybutadiene, these laminates have the dielectric constants range from 2.6-3.1 and their tan loss values from 0.3-0.9% (i.e. 0.003-0.009). Zussman in this case particularly chooses epoxy resin for the insulating resin layer (col 2 L 8-12).

The multilayer printed wiring board is made by laminating prepreg and copper sheet in alternating fashion. Then a device or an IC chip is mounted on the surface of the multilayer printed wiring board (col 6 L 18-24).

The examiner takes the position that the copper sheets formed wiring patterns which are embedded within the prepreg layers and that the copper foil on the outer surface forms a wiring pattern that connects to the embedded wiring patterns as well as the surface device (col 6 L 18-22).

Claim Rejections - 35 USC § 103

3. Claims 1-6 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zussman (US 4601944) in view of Berger et al (US 6528145) further in view of Hayashi (US 6359235) and Farquhar et al (US 6764748).

Art Unit: 1775

Zussman teaches the present invention but is silent about the water absorption of the insulating resin layer is equal to or less than 0.1% and the surface roughness of the patterned connecting line.

Berger discloses a multilayer printed circuit board which is used for mounting semiconductor devices (col 1 L 18-19).

The printed circuit boards are made of insulating layers such as glass filled BT/epoxy resins or ceramic filled liquid crystalline polymer, and wiring patterns are sandwiched between the insulating layers (col 5 L 41-42, L 45-46, L 65 & col 1 L 19-22, L 38-41).

The polymeric material has a dielectric constant of less than 3.5 and a moisture absorption rate of less than 1 % (col 5 L 29-33 & col 6 L 42).

The examiner takes the position that Berger's multilayer circuit board has the wiring patterns embedded within the insulating layers and having an exposed conductive surface (34) for electrical connection with a semiconductor device (col 12 L 44-46 & Fig. 3).

Hayashi and Farquhar both teach a structure of a multilayer printed wiring board with conductive patterns embedded within the insulating layers.

Hayashi's printed wiring board is coupled with a semiconductor device (col 5 L 64-66). The insulating layers are dielectric materials such as epoxy resin or bismaleimide triazine, etc. (col 4 L 59-67).

Farquhar chooses liquid crystal polymer material as the insulating layers for the multilayer printed circuit board (col 1 L 22-44).

In view of the prior art teachings, one skill in the art would choose either epoxy resin, bismaleimide triazine resin or liquid crystal polymer as dielectric material in making printed circuit boards because these resinous material are well known to possess better electrical properties (i.e. dielectric constant and dielectric loss), better moisture resistance, better dimensional stability and low cost, etc. benefits (see Hayashi, col 4 L 63-65 and Farquhar, col 3 L 43-45 & col 14 L 10-13).

The prior art are silent about the surface roughness of the connecting lines. Since applicant has not stated the less than or equal to 1 μm surface roughness is for any particular purpose, the examiner is taking the position that a surface roughness outside of this limitation would perform the same job.

Response to Arguments

4. Applicant's arguments filed on November 30, 2005 have been fully considered but they are not persuasive. Applicant argues that Zussman and none of the cited prior art teaches a semiconductor device with the claimed dielectric loss tangent value.

Zussman clearly teaches the dielectric and the tan loss value in the Table in column 7. The tan loss is a percentage (i.e. 0.1-0.9% refers to 0.001-0.009).

The examiner re-wrote the office action, such that it clearly addresses the issues raised in Applicant's remarks.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cathy Lam whose telephone number is (571) 272-1538. The examiner can normally be reached on 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Deborah Jones can be reached on (571) 272-1535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Cathy Lam
Primary Examiner
Art Unit 1775